MERGMODE Electronic Pailway Group TECHNICAL BULLETIN G16/8 Issue 1 Gordon Hopkins M328

FTC Floating Track Circuit

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Introduction.

One of the fundamental requirements for safe railway operation, both model and prototype, is that of knowing where the trains are. This information is essential if any form of interlocking and/or automation is to be implemented.

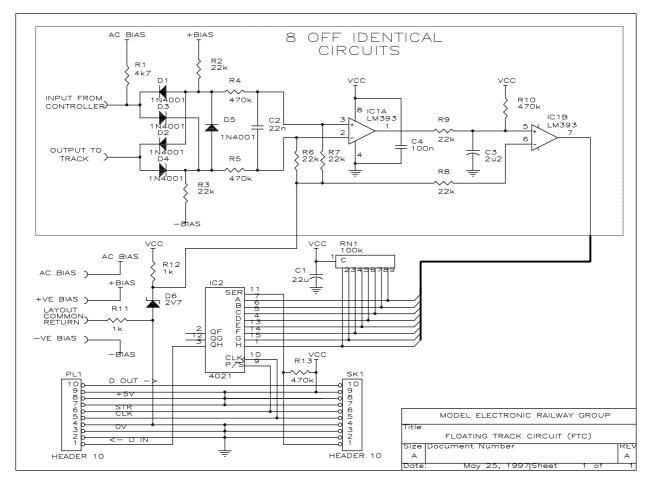
This circuit is designed to detect current flow through the 'Live Rail', rather than in the 'Return Rail' used in other designs such as the MERG ToTI. This has several advantages, not least of which is that only one rail need be broken for track sectioning, maintaining the advantages of true 'Common Return' wiring. Another advantage is the location of the entire circuitry within the Control Panel, minimising the wiring requirement, and allowing easy upgrade of layouts where the track circuit can be inserted 'in-line' with the existing wiring.

The module shown here provides eight independent live rail track circuits. The module is designed to be Control Panel mounted, as part of an RPC system.

Interface Specifications.

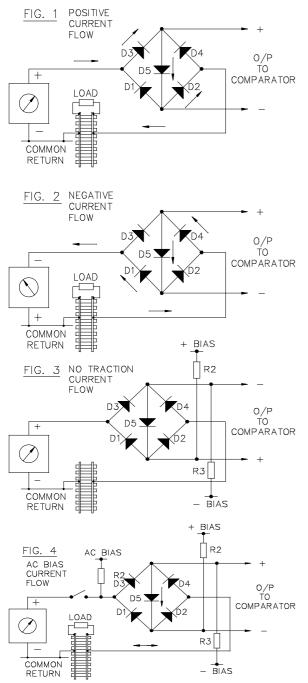
Power Requirement	o 11 y x
	+24V to +36V DC Bias.
	-24V to -36V DC Bias.
	AC Bias voltage (See Circuit Description).
Control Output	RPC Shift Register Compatible.
• Track Current Ca	pability 1A (Dependent on specification of diodes used).
Connectors	RPC Stacking plus 'Veropin' Terminals for layout wiring.
Logic Polarity	1 = Track Clear, 0 = Track Occupied.

Main Circuit Diagram.



Circuit Description.

D1 to D4 form a conventional bridge rectifier, with D5 connected across what are normally regarded as the d.c. output terminals.



Consider the case in Fig. 1, where the Controller Input is positive with respect to the Track, with a train in section. In this case, current flows from the Controller, through D3, through D5, then through D2 to the load (Train). This produces a positive voltage across D5 of one forward diode drop.

Alternatively, consider the case in Fig. 2, the Controller Input is negative with respect to the Track, current flows through the load, through D4, through D5, then through D1 to the Controller. This also produces a positive voltage across D5.

In order to detect the case where there is no load i.e. no train in section (Fig. 3), it is necessary to introduce some reverse bias to the diode network. The bias voltages must be at least as much as the Controller can provide at its output, preferably several volts more so that high values of bias resistors R2 & R3 can be used. High values of bias resistor are desirable to minimise the bias current and to limit their power dissipation as the Controller output swings from one extreme to the other.

The next possibility to contend with is when a Track Section is switched off, but there is a train present (Fig. 4). In this circumstance, an extra current source is needed as an alternative to the Controller. The ac bias source provides this facility. The voltage provided by this source needs to be similar in amplitude to the Controller maximum output, but less than or equal to the dc bias supplies. The current from the ac source must be high enough for reliable train detection, but low enough not to cause heating effects in the motor. If a dc supply were used for this task, there exists the possibility of finding a balance point, where the Controller current exactly matches that from the source, and the detection fails. In practice, this does not seem to be too much of a problem, as it could only occur at minimal Controller settings. This means that it is possible to use one of the dc bias supplies for the same job in most circumstances (usually the + bias). If the ac option is used, there is no particular frequency or waveform required. It is suggested that a square wave might be simpler to produce electronically, or a spare transformer winding of suitable voltage would suffice, giving a 50Hz sine wave. The only constraint on frequency is that its period should be lower than the time constant of the Comparator circuitry which follows.

Referring now to the main circuit diagram, the polarity of the voltage across D5 is detected by differential comparator IC1a, via attenuator network R4,5,6,7. This network provides approximately 20:1 attenuation of the incoming voltages, and is required to keep the Comparator input voltages within its supply rails. As the attenuation ratio is so high, these resistors are of 1% tolerance, as 5% types would give 1/20 variation of their own accord. C2 provides reasonable noise immunity by filtering out switching spikes generated by the layout. R12 and D6 set the attenuator reference voltage at approximately half the +5V rail, so that both positive and negative input excursions stay within the 0V to +5V range.

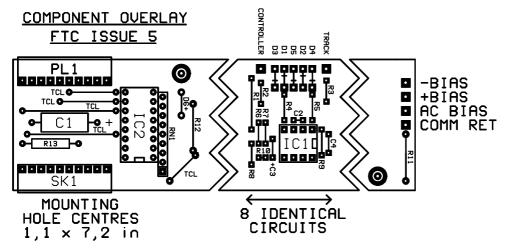
When a positive voltage is detected across D5 (Train in Section), the output of IC1a goes low. Capacitor C3 discharges via R9, and within 30ms the resulting voltage at IC1b pin 5 goes below the reference voltage on pin 6, eventually reaching approximately 0.25V, well below the reference. As a result, the output of IC1b goes to logic '0' (0V), which clears the associated input bit of shift register IC2.

When a negative voltage is detected across D5 (No Train in Section), the output of IC1a goes open circuit due to its open collector output stage. Capacitor C3 charges towards the supply rail via R10, and, after approximately 0.75s, the voltage at IC1b pin 5 is rises above the reference voltage on pin 6. As a result, the output of IC1b goes open circuit, and is pulled up by RN1 to logic '1' (+5V) and sets the input bit of shift register IC2.

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Thus, so long as there is a suitable current path through the diode network, a load connected across the track will be indicated by a logic '0' signal received back at the RPC Interface. This applies to each of the eight circuits located on the module. The eight bit signals are shifted out of the module by the RPC Interface using the standard RPC shift register stacking method.

Other components: C4 is the supply decoupling capacitor for IC1, C1 is the supply decoupling capacitor for the main RPC bus, R13 provides a pull-up on the shift register cascade input, and R11 provides a reference connection between the layout common return and the electronic circuitry 0V rail.

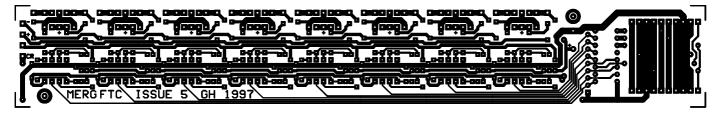


Parts List

Resistor Network Resistor Resistor Resistor Capacitor Capacitor Capacitor Capacitor Capacitor Rectifier Diode IC IC Zener Diode Header Plug Header Skt Veropins Spacers	10k x 8 1k 5% $\frac{1}{4}W$ 4k7 5% $\frac{1}{2}W$ 22k 1% W 470k 1% W 22n Ceramic 100n Ceramic 2.2µF 16V Tant 22µF 16V 1N4001 LM393N 4021B BZX55C2V7 10 pin R/A 10 pin R/A Single sided M3 Clearance x 4mm	1 off 2 off 8 off 48 off 25 off 8 off 8 off 1 off 1 off 1 off 1 off 1 off 1 off 20 off 2 off	RN1 R11,R12 R1 * R2,R3,R6,R7,R8,R9 * R4,R5,R10 * R13 C2 * C4 * C3 * C1 D1,D2,D3,D4,D5 * IC1 * IC2 D6 PL1 SK1 External Connections
Tinned Copper Wire	M3 Clearance X 4mm	As Reqd	Tinned Copper Links (TCL)

* These references apply to each of the eight circuits on the module.

PCB Track Layout (Not to Scale)



This Track Circuit design may be implemented in schemes other than the RPC system, and can be used in the same way as any other, whether as part of a signalling system or just with LEDs to show where the trains are. Future designs are envisaged which eliminate the need for the bias supplies, although these are no real hardship to produce, given the capabilities of the MERG Membership in these matters.